Battery Management System: Testing the EPC2001. Tyler Head[123], Edgar Cilio[2], and Washington Cilio[2], [1]University of Arkansas REU Program for Space and Planetary Sciences, [2]Arkansas Power Electronics Inc., and [3]Arkansas Tech University.

Introduction: The EPC2001 is a Gallium Nitride field effect transistor (GaN FET). [1] This GaN FET has high current–carrying and voltage-blocking capabilities (100-Amp pulses and 100 Volts, respectively), for its relatively small area, approximately four millimeters by one and half millimeters. [2] FETs are three terminal devices that work like a switch. A voltage is applied at the gate of the device (the control terminal) which allows a current to flow from the drain terminal to the source terminal. Once the voltage is no longer applied to the gate of the device, the current no longer flows.

The desired application for this GaN FET is to use it as a part of a switching power converter. The converter will process and manage the power flow from a bank of three batteries to a distribution bus. In order to be used, these FETs must be able to withstand at least 25 Amps (A) instantaneously and 50 Volts (V). To test the EPC2001, a clamped inductance test will be used.

Clamped Inductance Test: A clamped inductance test forces the power device to experience a worst-case switching transition condition. In this specific test, the EPC2001 will be tested above 25A and at 50V. The test is performed by applying a voltage to an inductor and diode in parallel that leads to the drain of the device, and the source of the device is at reference voltage. A microcontroller is attached to a gate driver which is then connected to the gate of the power device through a resistive network. The microcontroller outputs two pulses to the gate driver. One long pulse is applied to the gate first which creates the conduction channel from drain to source, allowing current to build in the inductor. Next, there is a pause between the two pulses. During this pause, the current circulates only in the inductor/diode loop. Then, a short pulse is applied to immediately discharge the high current in the inductor through the device. A capacitor bank is also used to help supply the instantaneous current to the inductor that the power supply might not be able to output.

Components: Most of the components used had to be purchased to fulfill specific requirements. However, the inductor, capacitor bank, measuring devices, and power supplies were already available.

Available Parts. The value of the inductor was measured to be 51 micro Henries with a 200 milliohm series resistance. The capacitor bank was measured at 230 micro Farads.

Parts Purchased: Most parts were purchased with twice the current and voltage capability necessary. Various resistors were purchased to enable optimization of the test setup. The diode in parallel with the inductor was purchased to withstand 200V and 120A. [1] The gate driver purchased, the lm5113, was recommended by the data sheet of the GaN FET. The microcontroller used was the C8051F410, which was determined to be able to provide the quick pulses required for this test. A zener diode was also purchased to be inserted right before the gate of this device to be used as a voltage regulator.

Simulations: The first step in this project was to run simulations to get a first-order approximation of how the device would respond to the set up described. A manufacturer-provided circuit model was used to simulate EPC2001's electrical behavior. The simulation aided in determining an estimate for each pulse's time length in order to reach the desired current level. The simulation was run at 50V at the capacitor bank, 5V pulses at the gate, and with the components at their previously mentioned values.

The first few sets of simulations completed were not completely accurate in comparison to the actual test because a few physical aspects were not taken into account. The accuracy of the simulation's results was improved once the power supply's impedance, capacitor bank, and series resistance of the inductor were included in the model.

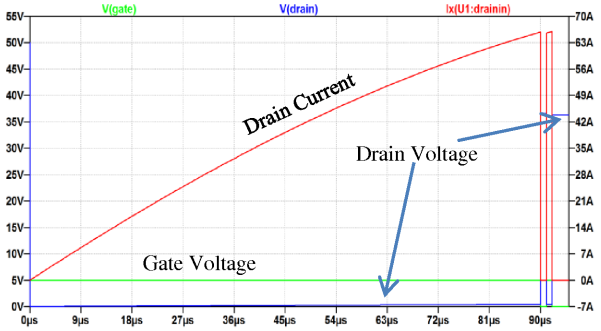

Figure 1: Clamped Inductance Test Simulation at 60Amps

The simulation above was run to yield a 60A drain current. At least 60A were desired because the printed circuit board (PCB) was designed for two paralleled GaN FETs to determine the current-sharing capability between two devices. The 60A total would provide 30A to each device, which is greater than the required current for the battery management system. Also, the simulation showed how one GaN FET responded to a current more than double to that necessary.

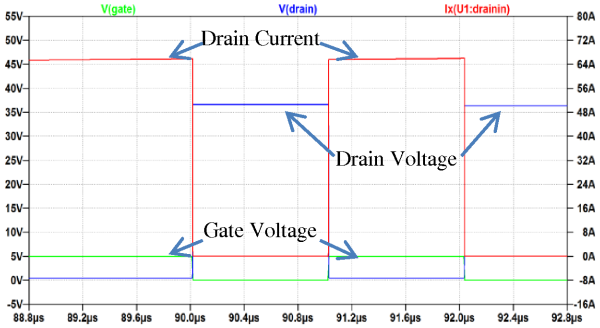

Figure 2: Simulation Zoomed in on the Second Pulse

Printed Circuit Board Design: The GaN FETs, gate driver, resistors, and capacitors were placed on a PCB designed for this test. The board also had separate inputs to the two GaN FET's drain and source, as well as an input and ground for both the gate driver and the input pulses from the microcontroller. The drain terminals for the two power devices were separate so they could be tested individually. The PCB had two layers. One was for all of the components, and the second was for a ground plate so all the components would have a common ground.

Physical Test: Once the PCB was populated and the microcontroller was programmed to the proper pulse lengths, the physical clamped inductance test was performed. The test worked very similarly to the simulation.

A few modifications had to be performed to reduce ringing and voltage spikes throughout the board. Two copper plates were installed. One was placed between the inductor and the drain of each device. The other plate was placed between the negative side of the capacitor bank and the source of each power device. This provided a lower resistance and less unclamped inductance than a regular wire. Also, a via had to be removed from the PCB by scratching out the connection because it created a ground loop. This caused one of the GaN FETs to respond differently than the other. More capacitance was also installed in the circuit where the gate driver was powered to reduce any fluctuation in voltage from the 5V power supply.

Once these modifications were done, the test was performed at 50V at the capacitor bank and 5V pulses at the gate as it was done in the simulation.

In Figures 3 and 4, the drain voltage still has a spike and ringing, but it has been greatly reduced with the modifications described. It can also be seen that the voltage is not at the full 50V. 50V was applied to the capacitor bank, but the power supply could not provide the current to maintain the voltage. This can also be seen in the simulations. More capacitance could be added to remedy this problem, but time and resources limited the ability to fix this immediately. However, the results are still highly relevant to the end application. The gate voltage shown is the input signal from the microcontroller. The two drain currents shown are the currents going through each GaN FET. Drain current 2 is the FET that is further from the inductor. It can be seen that the current is approximately 5A less than drain current 1 because there is more resistance in its path compared to the FET that is closer to the inductor.

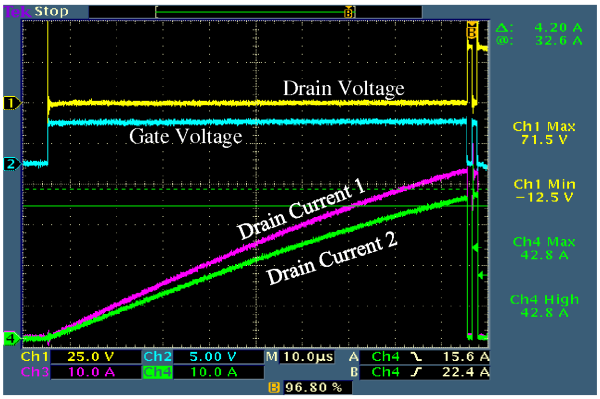

Figure 3: Physical Clamped Inductance Test Results.

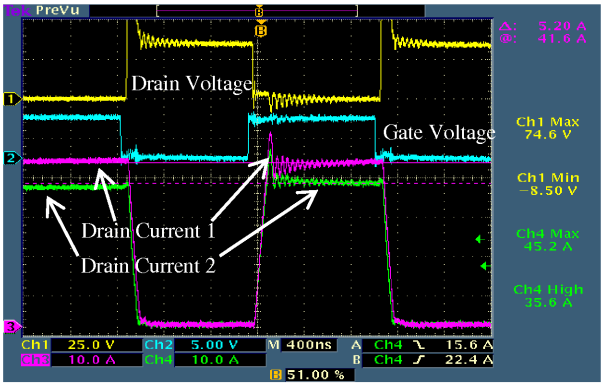

Figure 4: Physical Test Results Zoomed in on the Second Pulse

Conclusion: The EPC 2001 has proven to be a good candidate for switching in power electronics in a multi-device switch position arrangement. It has very fast switching capabilities, on the order of nanoseconds, and its data sheet specifications have been experimentally confirmed. After applying 50V, and over 30A through the EPC2001, it can be concluded that this GaN FET can be used in the battery management system.

References: [1] Efficient Power Conversion Corporation (2011) EPC2001, http://epc-co.com/epc/. [2] Mohan N., Undeland T. M., and Robbins W. P. (1995) Power Electronics, 571–595.

Acknowledgements: We gratefully acknowledge the National Science Foundation for sponsoring this work under grant No. 1157002. We also thank APEI, Inc. for providing technical direction and access to their facilities for the completion of this work