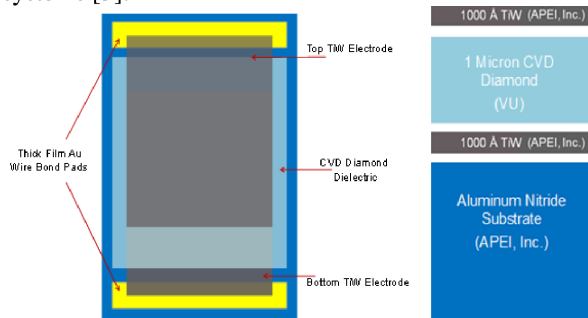


**EXTREME ENVIRONMENT CAPACITORS.** C. C. Flores<sup>1</sup>, J. R. Fraley<sup>2</sup>, L. E. Kegley<sup>2</sup>, and S. E. Minden<sup>2</sup>,  
<sup>1</sup>The University of Texas-Pan American, Edunburg, TX, <sup>2</sup>Arkansas Power Electronics International, Inc., Fayetteville, AR.

**Introduction:** Currently almost all space crafts are power-driven by chemical propulsion systems [1]. Due to high specific impulses as well as light weight propellant, nuclear thermal propulsion systems are becoming a more viable power option for future space exploration. NASA’s goal is to utilize nuclear thermal propulsion systems which would allow for rapid trips from Earth to Mars, significantly reducing mission times. In order to achieve such high efficiencies, NTP engines must function in hostile environments, experiencing radiation in their engine compartments and operating in extreme temperatures and pressures. Developing extreme environment electronics will enable sensing of crucial parameters within the NTP engine such as temperature, pressure, and neutron flux. Such sensors will provide the much needed engine health status as well as prognosis for future missions [1].

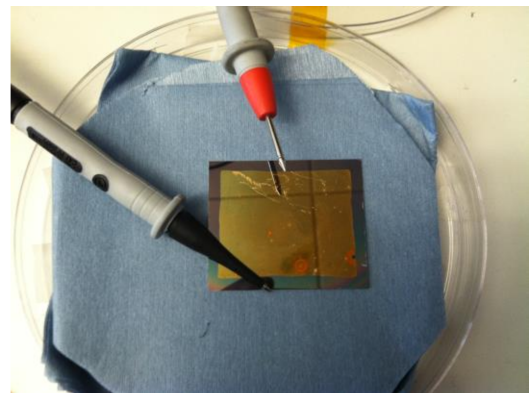
Being that capacitors are an integral part of any electrical system, it is important that they survive in an NTP environment. Arkansas Power Electronics International, Inc. is developing extreme environment capable capacitors to complement its high temperature semiconductors such as silicon carbide transistors.

**Methods:** Being that diamond has the highest dielectric breakdown strength of any known material (30 MV/cm), APEI will be utilizing diamond as the dielectric material. APEI working alongside Vanderbilt University to produce thin diamond films using a chemical vapor deposition process(CVD). CVD processes rely on chemical reactions rather than physical reactions to promote the growth of thin films by allowing reactive gases to pass over a heated substrate in a furnace [2]. The CVD process deposits diamond on a silicon wafer and then TiW and Au is metalized in a post-process sputtering cycle. CVD diamond is being utilized for its practical development into harsh environment sensor systems [3].



**Figure 1:** Framework of the substrates layers.

During this research, a p-doped silicon wafer was utilized as a sturdy, conductive substrate. 5000 nm of CVD diamond was deposited on the silicon wafer, followed by a proprietary metal adhesion layer followed by a layer of gold. In this manner, a conductor/insulator/conductor parallel plate capacitor was formed. The researchers then measured capacitance, voltage blocking, and other parameters of the diamond capacitors at temperatures up to 500°C (932°F).

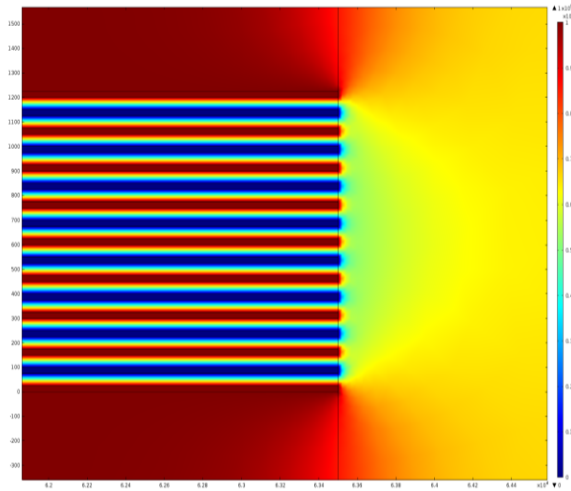


**Figure 2:** Displays an electronic measuring instrument.

**Results & Discussion:** Etching the capacitor, a process in which the wafer was immersed in a bath of etchant, chemically removing the metal adhesion and Au layers from the surface allowing for key measurements to be taken. The measured values however displayed a discrepancy in experimental values to the expectant values. The dielectric was behaving as a short circuit therefore defeating its purpose. Knowing the atmosphere that the diamond thin film was deposited in, there was awareness of the possible complications that might arise due to this atmosphere/temperature/etc. Specifically, it is hypothesized that what was encountered was a consequence of constituent parts of the carrier gas (hydrogen) getting trapped in the crystal lattice structure of the diamond film as it was growing on the silicon wafer. These hydrogen atoms were affecting the resistivity of the diamond film. The hydrogen atoms were allowing current to flow through the diamond film, making it a slightly conductive layer rather than the extremely nonconductive layer as expected. Putting it through an annealing process allowed the lattice structure to relax and for the hydrogen atoms to migrate out of the diamond thin film.

**Conclusion:** Allowing the diamond thin film to undergo the heat treatment of annealing for two hours

at 750°C (1382°F) altered its physical properties from a short circuit to an open circuit. This was proven by once again performing measurements of resistance and capacitance. Further work is being researched and conducted on creating multiple thin (sub-micron) dielectric layers through the CVD process as well as investigating the behavior of the electric field as it forms around the dielectric/air/etc.



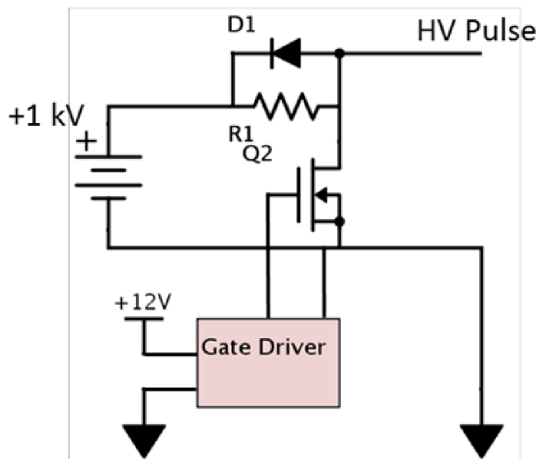
**Figure 3:** Surface electric potential of a dielectric.

**References:** [1] Extreme Environment SiC Wireless Sensor Suite for Nuclear Thermal Propulsion Engines. Proposal No: X2.03-9748. Topic: X2.03 [2] Ulrich, Richard and William Brown. Advanced Electronic Packaging. (2006) IEEE, 81-88. [3] Fraley, J. et al. High Temperature Hybrid NanoDiamond Sensor Systems.

**Acknowledgements:** This project was supported by the Arkansas SPAC program, with grants from the National Science Foundation- NSF #1157002 as well as NASA's Phase 2 SBIR contract award #NNX12CA30C. We also thank Vanderbilt University for collaboration on the diamond thin films as well as the extraordinary employees at APEI for their incredible support and assistance on this project.

**Introduction:** Working alongside Army Research Lab, Arkansas Power Electronics International, Inc. is working towards developing high voltage power conversion systems. Utilizing these high voltage systems will allow the army to increase the density and capability of power electronics used to power and control its vehicles. APEI will utilize silicon carbide electronics to enable for these high voltage systems. Polymer dielectric potting materials are used to isolate large potential differences inside a high voltage module. The modules being built by APEI are designed to be very power dense; a result of this is that the modules operate at a very high temperature. As the temperature of the potting compounds go up, the dielectric strength of them may go down. Building a system that can be used to test their properties will prove beneficial as there is no published data for how they behave at high temperatures.

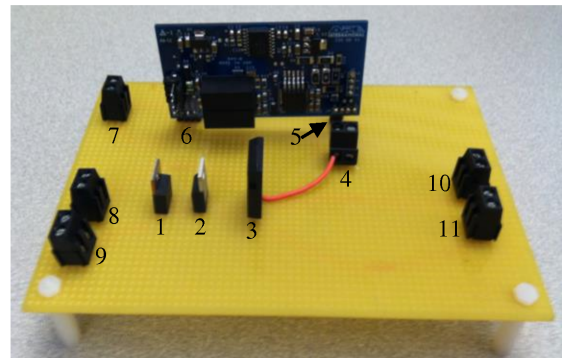
**Methods:** A 8 x 6 x 3.5 in. aluminum box with the addition of three input and two output holes was used as the enclosure of the high voltage testing box. The box will produce an output of 1kV, with an AC frequency of 2.78 kHz, and a voltage rise time of 40.9 V/ns.



**Figure 1:** dv/dt test box schematic

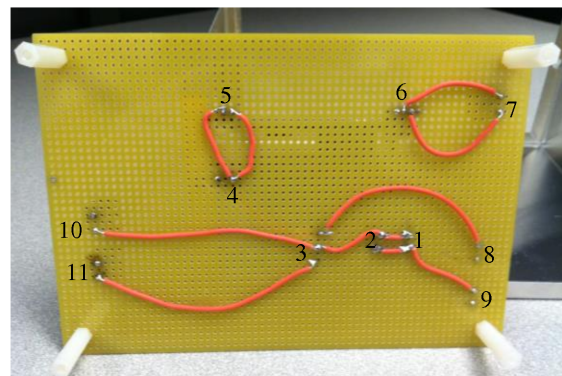
In order for the HV testing box to operate properly to the preset output value, the circuit must follow the (fig 1) schematic presented above. A high voltage direct current will be the input connection to both the resistor (1) which will be placed in parallel with the

diode (2) connecting to the drain of the mosfet (3), while producing an output HV pulse (10). The source of the mosfet (3) will have a ground output (11) as well as an input connection (8). The gate of the mosfet (3) will connect to terminal block (4) splitting connection to the gatedrivers source and gate (5). The gatedrivers 12V and ground (6) will link to terminal block (7) and also serve as an input connection for the circuit.



**Figure 2:** The translated SPICE schematic of electrical components and contacts to the perforated board.

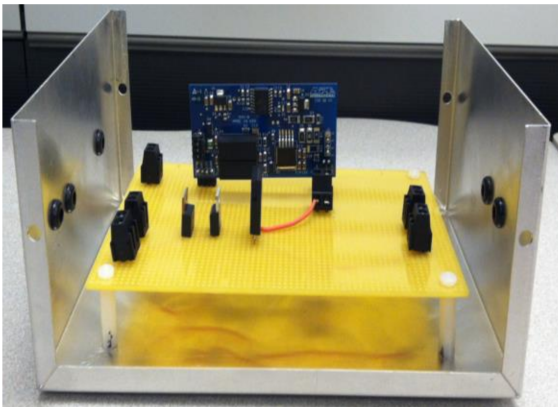
These electrical components (fig 2) are secured to a non-plated through hole perforated board for the purpose of not causing electrical arcs due to the high amount of voltage usage. Where each component made contact on the perforated board, they were soldered to pads as to ensure electrical isolation. Connections were made with a variety of techniques including wire wrap, metal socket strips, and soldering as seen in (fig 3) making a strong electrical and mechanical connection.



**Figure 3:** Displays the soldering connections between the electrical components.

**Results & Discussion:** Early in the project a 1 kV pulse generator was built to facilitate the dv/dt testing

of dielectrics. It created a pulse with a  $dv/dt$  of 40  $kV/\mu s$ . Initial tests showed that the voltage transitions were too fast for our equipment to resolve. A modification of the power supply was conceived and is currently being implemented. An additional box was conceived to create a consistent and measurable voltage signal. The original box used the control circuitry of a boost converter to generate a high  $dv/dt$  signal. This however did not create a consistent signal and was difficult to measure. This new box (fig 5) creates a similar high  $dv/dt$  signal using a resistor in series with a similar MOSFET as used in the original box. The output of this new box is taken between a resistor and a MOSFET. This signal is controllable via an external signal such as a PWM generator which is fed into a gate driver that controls the MOSFET. This allows for a viable frequency signal that is both measurable and consistent while maintaining a high  $dv/dt$ .



**Figure 5:** HV testing box.

**Acknowledgements:** This project was supported by the Arkansas SPAC program, with grants from the National Science Foundation- NSF grant #1157002. We also thank the Army Research Labs for collaboration and funding of this project as well as the extraordinary employees at APEI for their incredible support and assistance on this task.